Advanced Microelectronic Front End Processes, Transistors, and Back End Processes Challenging the Modeling and Simulation of the Semiconductor Processes and Devices

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The presentation will give a general overview about advanced microprocessor technologies. The international technology roadmap of semiconductors is used to guide the process and device simulation community through the requirements for FEOL processes, transistor formation, and BEOL processes.

Sub-50 nm SOI technologies are mature at AMD and run in high-volume production. Advanced modules of these technologies are shown to illustrate and to define challenges for the modeling and simulation of semiconductor processes and devices. Appropriate examples are the shallow trench isolation, the manufacturing of ultra-thin gate dielectrics, the gate pattering, and the Cu interconnect using CVD-deposited low-k dielectric.

Forecasting further extendibility and process developments, future requirements for the process and device simulation will be outlined. This is a joint work with G. Burbach, T. Feudel, D. Greenlaw, M. Horstmann, P. Hübler, T. Kammler, S. Krügel, M. Lenski, K. Romero, K. Wieczorek and M. Raab.